Data sheet

Version 01.00

September 2004

R&S®In-Circuit Test Option for R&S®CompactTSVP

using R&S®TS-PSAM, R&S®TS-PICT, R&S®TS-PMB and Software R&S®TS-LEGT, R&S®TS-LEG2

- Complete analog in-circuit measurement unit with R&S®TS-PSAM and R&S®TS-PICT
- Test of R, L, C, diodes, transistors, parallel R-C
- Guarded resistor measurements (3-, 4-, 6-wire)
- Guarded impedance measurements (3-, 4-, 6-wire)
- Measurement frequencies 100 Hz, 1 kHz, 10 kHz for impedance tests
- Low stimulus voltage for isolation of diodes and ICs
- Test system based on CompactPCI, PXI and CAN
- Up to 300 tested parts per second
- Automatic test generator with circuit analysis and testability check
- Standard interface for CAD data import
- Easy-to-use EGTSL environment for in-circuit test debugging
- Up to 900 test pins in single-chassis R&S®CompactTSVP
- Up to 2250 test pins in dual-chassis R&S®CompactTSVP/R&S®PowerTSVP solution

ROHDE&SCHWARZ

Product introduction

Continuing the R&S®CompactTSVP product family's philosophy of scalability and flexibility, a modular and cost-effective in-circuit test (ICT) platform can also be easily created using hardware and software from the R&S®CompactTSVP product portfolio.

The R&S®ICT Option provides a wide variety of standardized test methods and combinations. To meet each customer's requirements, the classic analog ICT can be merged with all functional tests (FCT) offered by the R&S®CompactTSVP family as well as with the entire spectrum of products from the PXI and cPCI market.

The R&S®ICT Option is based on the CompactPCI measurement and stimulus modules R&S®TS-PSAM and R&S®TS-PICT. Each module takes up only one slot in the R&S®CompactTSVP and has a floating power supply as a rear I/O module. The R&S®TS-PICT expands the Analog Source and Measurement Module R&S®TS-PSAM to provide fully analog ICT capability. In ICTs and FCTs, the DUT's test pins are routed via the Switching Matrix Module R&S®TS-PMB and the Rohde&Schwarz measurement bus to the R&S®TS-PICT and R&S®TS-PSAM measurement units. Therefore, the same test pins can be used for ICTs and FCTs. A standardized fixture interface (R&S®TS-PAD3/ R&S®TS-F3F), directly mounted on the R&S®CompactTSVP chassis, provides high signal quality to the fixture.

Typical applications

Since the ICT functionality is divided into different modules, the modular ICT option can be precisely configured to the customer's requirements. Applications may vary from an FCT enhancement to a classic analog ICT solution.

The ICT expansion provides the following benefits, especially for the FCT:

- A contact test checks whether the contacts with the DUT (wiring test) are functioning properly
- A shorts test prevents the DUT or the test system from being destroyed during power-up
- A continuity test detects open signal paths

When the modular ICT option is used, even a full ICT system can be configured, thus providing the following features:

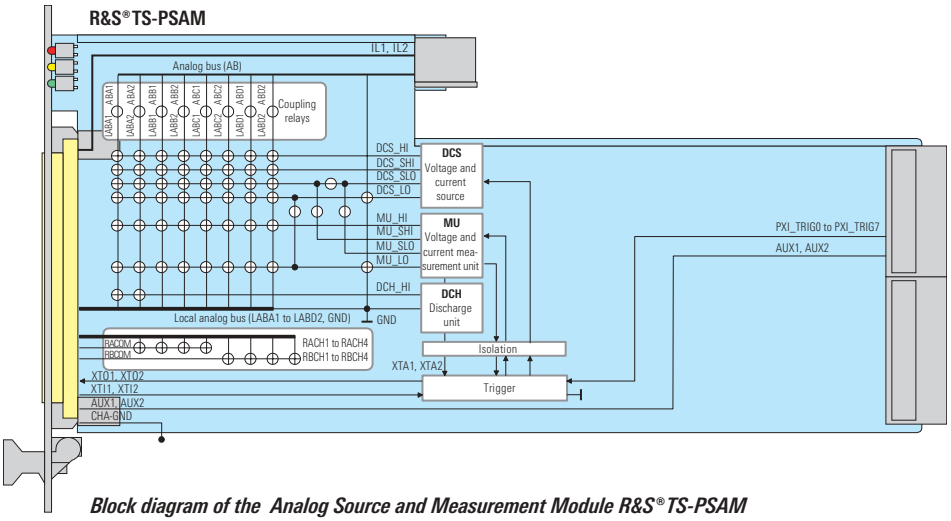
- Automated test generation
- Highest flexibility in terms of scalability and functionality
- Excellent test speed
- State-of-the-art graphics-based debugging environment

In addition, the implementation of the industry standards PXI and CompactPCI ensures that FCT methods can be added regardless of vendor.

Hardware

For ICTs, the following measurement tasks are performed by the R&S®TS-PSAM:

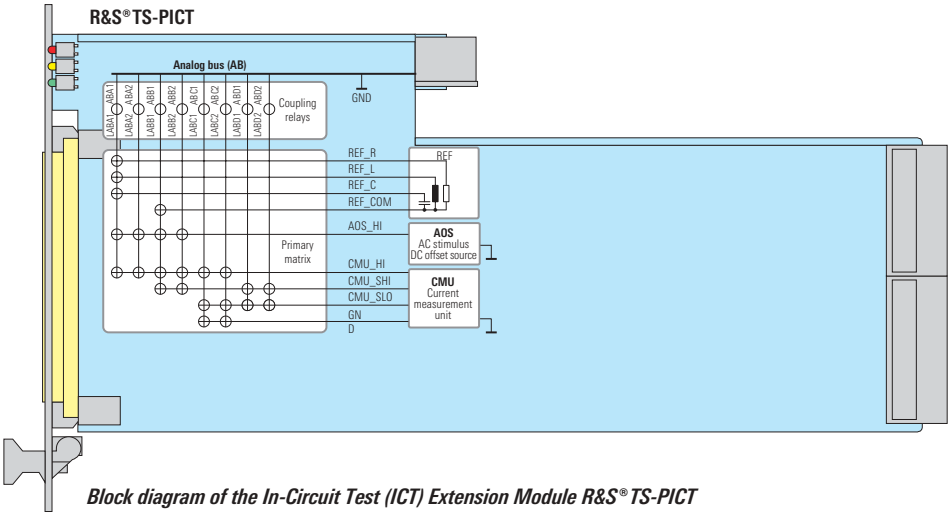
- Discharge of capacitors and printed boards
- Contact test
- Shorts test
- Continuity test
- 2-wire and 4-wire resistance measurements (DC)
- Measurement hardware for system selftest



Block diagram of the Analog Source and Measurement Module R&S®TS-PSAM

In addition, the R&S®TS-PSAM covers essential FCT requirements:

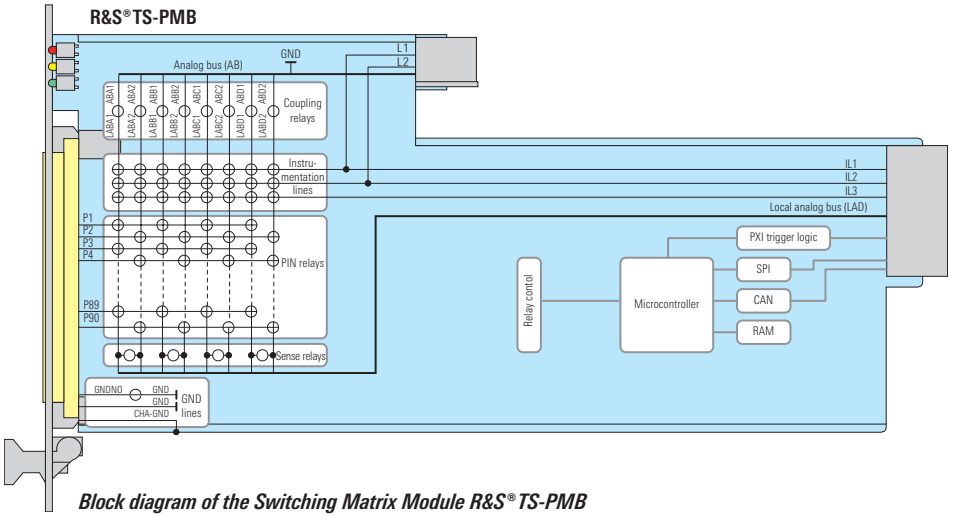
- Current/voltage measurement
- Data acquisition (i.e. waveform recording)
- Trigger/clock generation



Block diagram of the In-Circuit Test (ICT) Extension Module R&S®TS-PICT

In conjunction with the R&S®TS-PICT, guarded measurements can also be performed:

- Resistor, capacitor, inductor (AC) tests
- 3-, 4- and 6-wire resistance (DC) and impedance measurements (AC)
- Diode and transistor tests

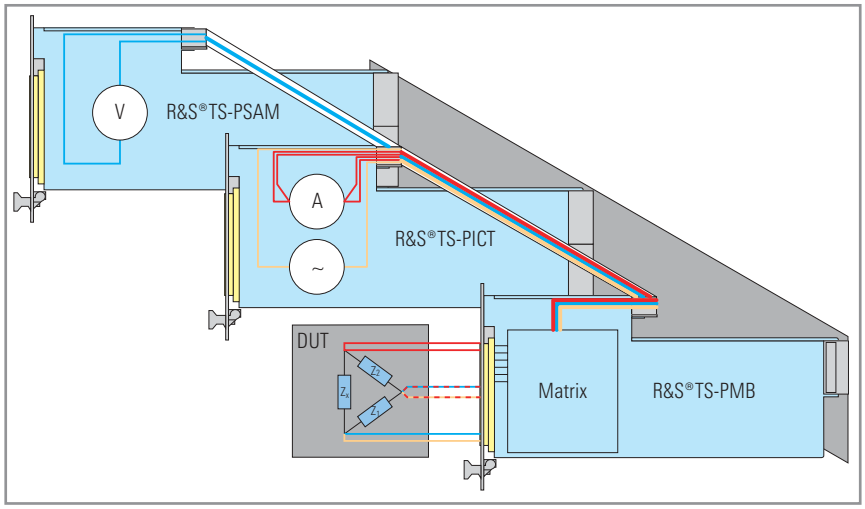


Block diagram of the Switching Matrix Module R&S®TS-PMB

Wiring the adapter is simplified by the full matrix of the Switching Matrix Module R&S®TS-PMB in the case of 2-wire and 4-wire techniques. This module is controlled by the controller area network (CAN) bus, which has already proven itself to be a rugged bus system in the automotive market. The pin count is scalable in steps of 90 pins.

In highly complex test cases, the combined use of all modules yields a highly sophisticated virtual instrument. The R&S®CompactTSVP backplane links the different modules together with CAN, cPCI and PXI buses. The analog measurement backplane is separated from the digital backplane to provide high-quality and reproducible analog signal routing.

Parallel components in a DUT circuit and test system residuals are compensated for by using guarding, sensing and phase-correct measurement technology.



Schematic diagram of a guarded impedance test

Software

ICT programs are generated automatically by the Automatic Test Generator (ATG), which creates a test proposal in XML format directly from the CAD data interface (BDL file format).

Flow chart of the ICT program generation

The well-structured graphical user interface, which is highly intuitive for anyone with experience in Windows-based applications, makes debugging and optimization quick and easy.

The high-speed tests, typically only 3 ms per part, are performed using a special precompiling algorithm of the Enhanced Generic Test Software Library (EGTSL).

This algorithm analyzes the test sequence and generates very efficient meta-code when saving the program (e.g. optimization of range switches, selection of bus lines).

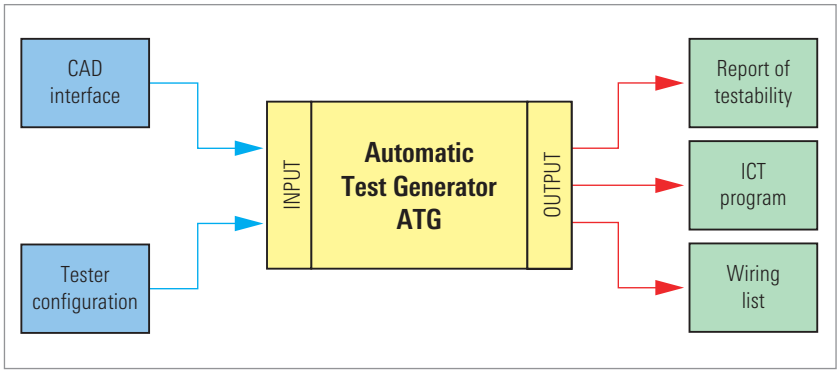
The simple execution of the ICT runtime via DLL calls from any sequencer software ensures flexible and straightforward integration into the software environment.

The ICT program is implemented in the FCT like a normal test step.

The R&S®TS-LEG2 software, which is a subset of R&S®TS-LEGT, supports the basic ICT functions. These functions can be performed only by the R&S®TS-PSAM (discharge, contact, shorts, continuity, 2-wire and 4-wire resistance).

Automated test generation

ICT programs are generated automatically by the Automatic Test Generator (ATG). The ATG analyzes the DUT circuit described in CAD data (BDL file format). Appropriate test and guard points are selected automatically. Test requirements and available tester configurations are compared, and resulting testability problems are reported. An executable ICT program that can be run by EGTSL is generated. The wiring of the DUT can be started immediately using the wiring file that has been created.



Program generation by the Automatic Test Generator (ATG)

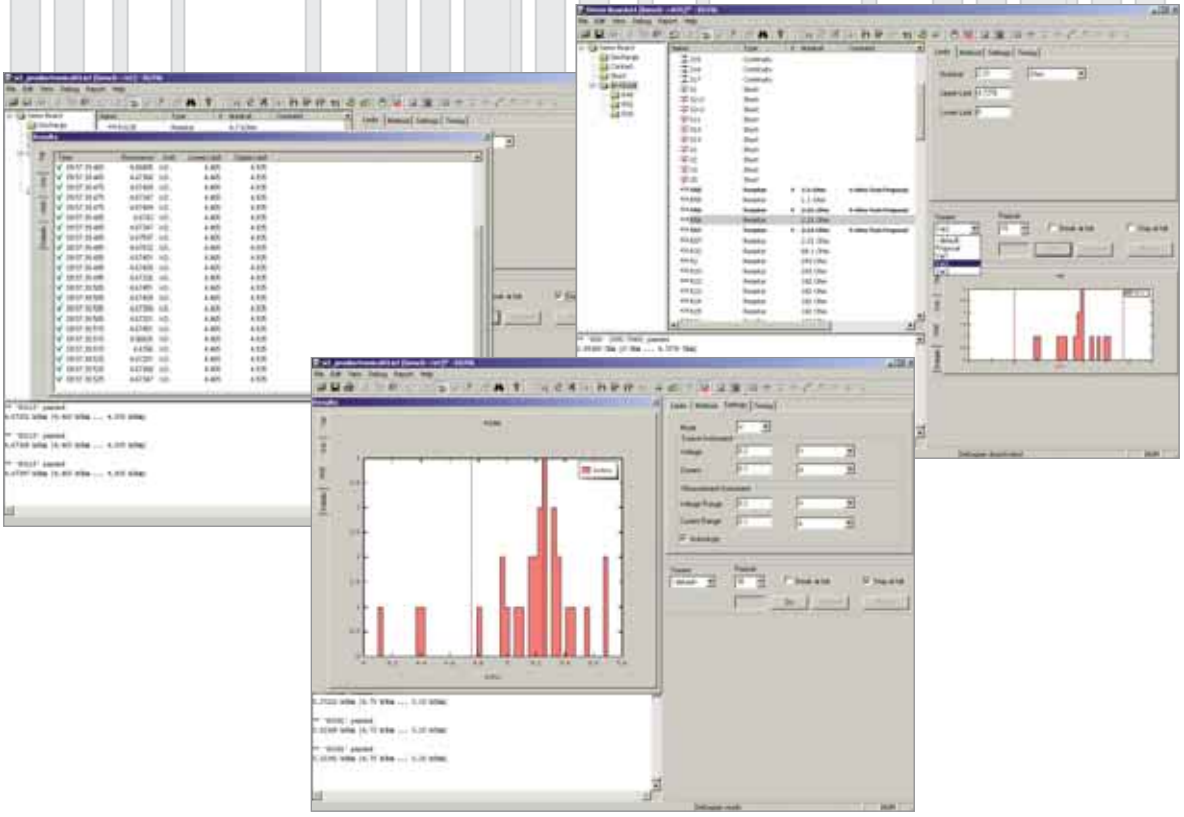
Debugging environment

The EGTSL debugging environment has the familiar look of modern Windows applications. With this graphical user interface, virtually anyone can quickly master the full spectrum of functionality and settings provided by EGTSL. There is no need to learn a special programming language or work with a predefined screen layout. Test engineers can create their own desktop and display all required information on one screen. They can scale, move, and display the windows as needed.

Even implementing a new test step is like creating a new folder in Windows Explorer, whose tree structure is similar to the ICT program flow in EGTSL.

Within the EGTSL debugging environment, users can do the following:

- Create, delete or move test steps by a mouse click or drag and drop
- Change settings of test steps, e.g. limits, test method, stimuli and measurement
- Define specific timing models
- Use compiler functionalities such as setting breakpoints, step into or over certain test steps
- Define and handle different variants
- Export and import limits
- Use statistical tools such as histograms to verify stable results
- Display a detailed test report
- Create the core program for the panel test



EGTSL debugging environment

Execution/Runtime

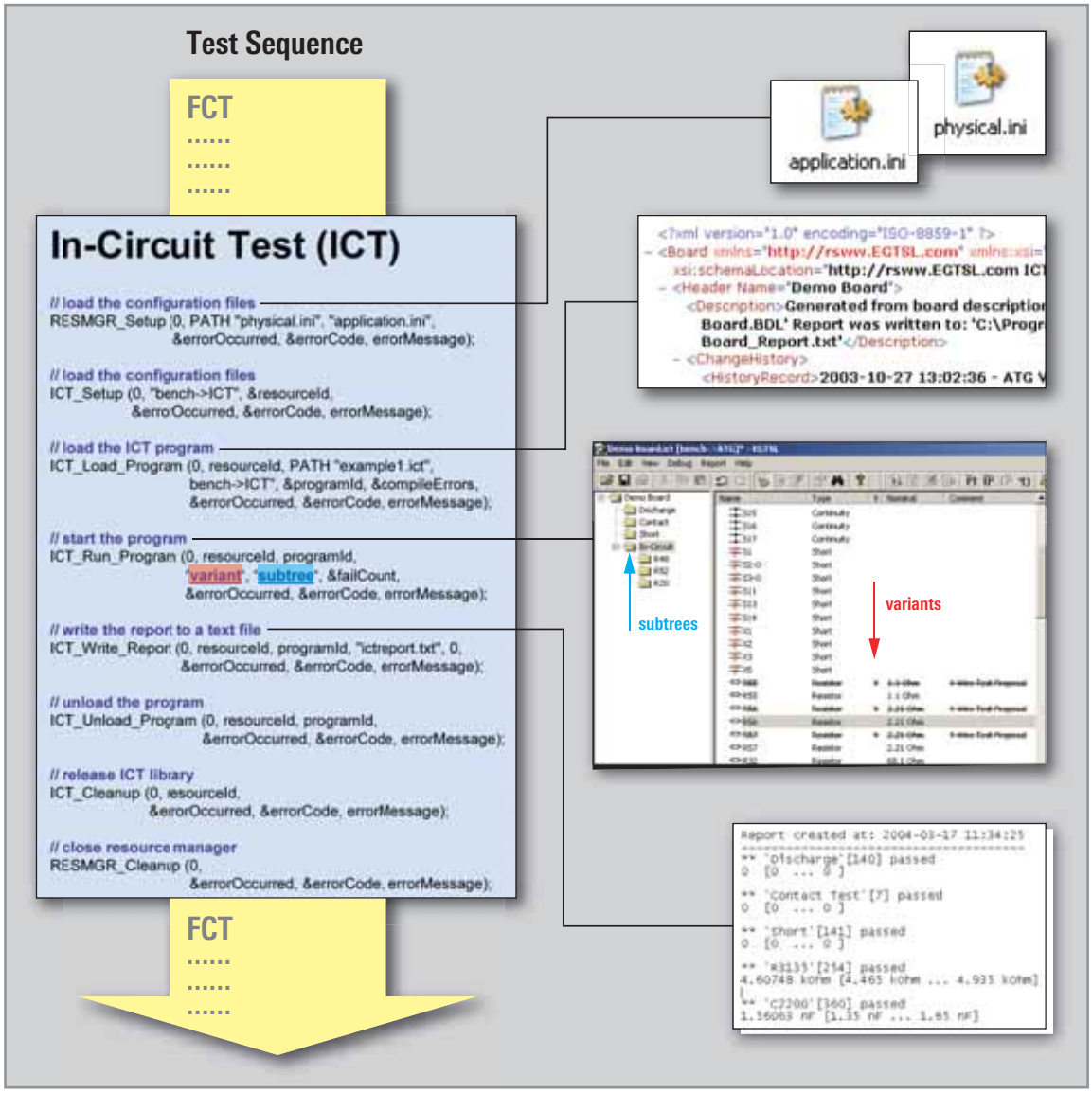
A separate sequencing program for the ICT option from Rohde & Schwarz is not needed. The ICT runtime can directly handle the customer's sequencer software, already used in the FCT.

The EGTSL is executed by a DLL call from the test sequencer (e.g. off-the-shelf test sequencer or dedicated executable software).

The test hardware is automatically managed by the resource manager, which handles the information available in the tester configuration files (PHYSICAL.INI and APPLICATION.INI).

Special failure routines or variant settings are covered by the entire functionality of the sequencing program. Therefore, each time a DLL call is performed, variants defined in the ICT program can be selected and each subtree can be executed independently.

A complete test result containing the information of the ICT and FCT can be generated by the sequencer due to handover of the ICT failure count. Additionally, a detailed ICT report can be generated.



ICT program integrated into a functional test

Configurations

A single-chassis R&S®CompactTSVP (R&S®TS-PCA3) can be configured with up to 900 test pins (ten R&S®TS-PMB modules). A dual-chassis configuration can provide an additional 1350 test pins with up to 15 Switching Matrix Modules R&S®TS-PMB in the R&S®PowerTSVP (R&S®TS-PWA3), yielding a maximum of 2250 test pins.

Several test system configurations are possible:

- "One box" ICT with up to 900 test pins and classic analog ICT functionality
- "One box" FCT/ICT solution with a mixture of FCT and ICT modules
- Dual-chassis FCT/ICT test system with measurement modules in the R&S®TS-PCA3 and switching modules up to 1350 pins in the R&S®TS-PWA3; DUT fixturing via the R&S®TS-PWA3
- Dual-chassis ICT with up to 2250 pins and full analog ICT functionality

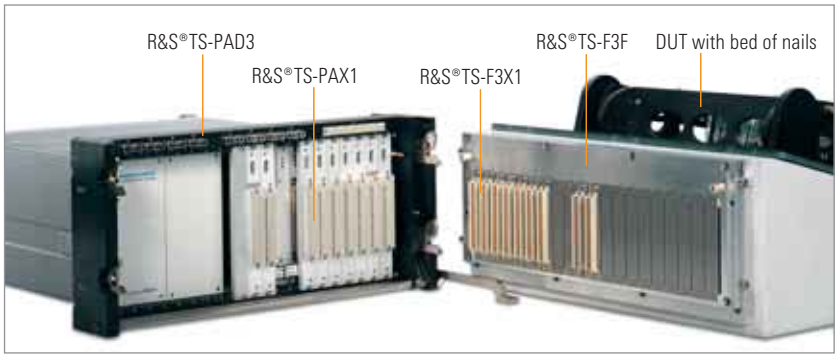
Combination of the R&S®TS-PWA3 and R&S®TS-PCA3 to form a fully analog ICT with 2250 pins

For all dual-chassis configurations, the R&S®CompactTSVP and R&S®PowerTSVP have to be connected via the analog measurement bus extension cable (R&S®TS-PK01) and the CAN bus control cable (R&S®TS-PK02).

Test fixture accessories

To accelerate integration of the R&S®CompactTSVP into production test environments in a quick and cost-effective manner, an entire set of mass-interconnection support products has been created. The platform modules are equipped with a 96-pin DIN 41612 connector which is easy to handle in fixture wiring using wire-wrap techniques.

The interface between the Receiver Frame R&S®TS-PAD3 and the Fixture Frame R&S®TS-F3F is provided by the modular Connector Carriers R&S®TS-PAX1 on the test instrument side and the Connector Carriers R&S®TS-F3X1 on the fixture side. Optional, spring-loaded precision contacts can be mounted.



Test fixture accessories

A vacuum control unit (R&S®TS-PVAC) with single or dual vacuum ports is directly controlled by the R&S®CompactTSVP.

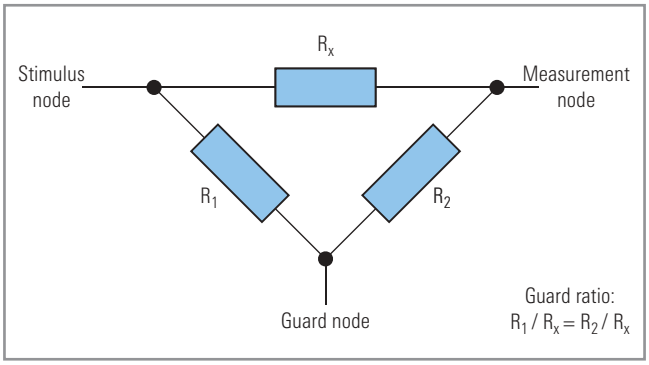
Security through selftest and diagnostic features

The built-in selftest capabilities range from fast diagnostics to complete, automated evaluations of all relays and switch paths. The use of the R&S®TS-PSAM allows a fast and comprehensive "in-system" selftest to be performed.

Diagnostic LEDs on the module front panel speed up installation and immediately indicate proper operation.

Specifications

Application in R&S®CompactTSVP / R&S®PowerTSVP	
R&S®CompactTSVP	one slot for R&S®TS-PSAM one slot for R&S®TS-PICT up to ten slots for R&S®TS-PMB
R&S®PowerTSVP (optional)	up to 15 slots for R&S®TS-PMB
Interface	
Control bus	CompactPCI/PXI bus CAN 2.0B for R&S®TS-PMB
DUT connector (front)	DIN 41612, 96 pins on R&S®TS-PSAM, R&S®TS-PMB
Tolerances of specified values apply under the following conditions:	
Recommended calibration period	1 year
Temperature range	23 °C ±5 °C
Additional error specified by the temperature coefficient in the range	5 °C to 18 °C and 28 °C to 40 °C



Resistor test, guarded

Resistor tests (DC)

Resistor test, non-guarded (R&S®TS-PSAM)

Range	Error limit	Source voltage (minimum)	Source current (minimum)	Mode [1]	Wires	Average	Sample interval
0.1 Ω to 1 Ω	1.0 + 5.0 mΩ [2]	0.5 V	100 mA	C	4	20	1 ms
1 Ω to 10 Ω	1.5 [3]	0.2 V	10 mA	C	4	20	1 ms
10 Ω to 100 Ω	0.5 [3]	0.2 V	25 mA	V	4		
100 Ω to 1 kΩ	0.5 [3]	0.2 V	2.5 mA	V	4		
1 kΩ to 10 kΩ	0.5 [3]	0.2 V	1.0 mA	V	2		
10 kΩ to 100 kΩ	1.0 [3]	0.2 V	0.1 mA	V	2	100	5 µs
100 kΩ to 1 MΩ	1.0 [3]	1.0 V	0.1 mA	V	2	20	1 ms
1 MΩ to 10 MΩ	1.0 [3]	5.0 V	0.1 mA	V	2	20	1 ms

[1] C = current injection, voltage measurement.
V = voltage injection, current measurement.
[2] Error limit: ±(% of reading + absolute value).
Temperature coefficient: ±(0.1 × accuracy) / °C.
[3] Error limit: ± % of reading.
Temperature coefficient: ±(0.1 × accuracy) / °C.

Resistor test, guarded (R&S®TS-PSAM, R&S®TS-PICT)

Guard ratio (R_1: R_x, R_2 : R_x)	Error limit [1]	Range (R_1 and R_2)	Source	Mode [2]	Wires
1 : 1	0.5	10 Ω to 100 Ω	0.2 V	V	6
1 : 10	1.0	10 Ω to 100 Ω	0.2 V	V	6
1 : 100	1.0	10 Ω to 100 Ω	1.0 V	V	6
1 : 1000	7.0	10 Ω to 100 Ω	1.0 V	V	6
1 : 1	0.5	100 Ω to 1 kΩ	0.2 V	V	6
1 : 10	0.5	100 Ω to 1 kΩ	0.2 V	V	6
1 : 100	1.0	100 Ω to 1 kΩ	1.0 V	V	6
1 : 1000	7.0	100 Ω to 1 kΩ	1.0 V	V	6

[1] Error limit: ± % of reading.
Temperature coefficient: ±(0.1 × accuracy) / °C.
[3] V = voltage injection, current measurement.

Impedance tests (AC)

(R&S®TS-PSAM, R&S®TS-PICT)

Notes:

The system residuals caused by the test system and the wiring in the fixture must be taken into account for all impedance measurements. Especially the parasitic capacitance has an influence on the measurement of large resistors, large inductors and small capacitors at a high frequency. The major part of the capacitance is compensated for by a software correction process that considers the actual system configuration. The remaining deviation (typically 0 pF to 30 pF) must be taken into account dependent on the actual interface connection with the DUT.

The error limits are increased to factor 2 in the case of stimulation with offset.

The error limits for capacitance and inductance are valid for a figure of merit ≥6, i.e. for a phase angle in the range of ±(90° ±10°).

Resistor test AC (non-guarded)

Measurement frequency 100 Hz			
Range	**Error limit [1]**	**Source (AOS)**	**Measurement method [2]**
1 Ω to 6 Ω	1.2	0.2 V	V 4-wire
6 Ω to 60 kΩ	0.7	0.2 V	V 4-wire up to 100 Ω
60 kΩ to 300 kΩ	1.2	0.2 V	V
300 kΩ to 1 MΩ	1.2	1.0 V	V

Measurement frequency 1 kHz			
Range	**Error limit [1]**	**Source (AOS)**	**Measurement method [2]**
1 Ω to 6 Ω	1.2	0.2 V	V 4-wire
6 Ω to 60 kΩ	0.7	0.2 V	V 4-wire up to 100 Ω
60 kΩ to 300 kΩ	1.2	0.2 V	V
300 kΩ to 1 MΩ	1.2	1.0 V	V

Measurement frequency 10 kHz			
Range	**Error limit [1]**	**Source (AOS)**	**Measurement method [2]**
3 Ω to 20 kΩ	1.2	0.2 V	V 4-wire up to 100 Ω
20 kΩ to 100 kΩ	2.2	0.2 V	V [3]

Capacitor test (non-guarded)

Measurement frequency 100 Hz			
Range	**Error limit [1]**	**Source (AOS)**	**Measurement method [2]**
1 nF to 20 nF	1.0	U: 1.0 V	V
6 nF to 100 nF	1.2	U: 0.2 V	V
0.1 µF to 200 µF	0.7	U: 0.2 V	V 4-wire for ≥100 µF
200 µF to 1000 µF	2.0	U: 0.2 V	V 4-wire
1000 µF to 10000 µF	5.0	U: 0.2 V	V 4-wire

Measurement frequency 1 kHz			
Range	**Error limit**	**Source (AOS)**	**Measurement method [2]**
100 pF to 1000 pF	1.2 + 2.0 pF [4]	1.0 V	V
0.6 nF to 10 nF	1.2 + 2.0 pF [4]	0.2 V	V
0.01 µF to 1 µF	0.7 [1]	0.2 V	V
1 µF to 10 µF	1.0 [1]	0.2 V	V

Measurement frequency 10 kHz			
Range	**Error limit**	**Source (AOS)**	**Measurement method [2]**
10 pF to 220 pF	1.0 + 2.0 pF [4]	1.0 V	V [3]
220 pF to 1000 pF	0.7 + 1.0 pF [4]	1.0 V	V [3]
1 nF to 22 nF	0.7 [1]	1.0 V	V
60 pF to 1000 pF	1.0 + 2.0 pF [4]	0.2 V	V [3] average 5
1 nF to 200 nF	1.2 [1]	0.2 V	V

Inductance test (non-guarded)

Measurement frequency 100 Hz			
Range	**Error limit [1]**	**Source (AOS)**	**Measurement method [2] [5]**
1 mH to 20 mH	3.0	0.2 V	V
20 mH to 30 H	2.0	0.2 V	V
30 H to 100 H	5.0	0.2 V	V

Measurement frequency 1 kHz			
Range	**Error limit [1]**	**Source (AOS)**	**Measurement method [2] [5]**
250 µH to 2 mH	3.0	0.2 V	V
2 mH to 3 H	2.0	0.2 V	V
3 H to 10 H	2.0	0.2 V	V

Measurement frequency 10 kHz			
Range	**Error limit**	**Source (AOS)**	**Measurement method [2] [5]**
60 µH to 1 H	2.0 [1]	1.0 V	V
25 µH to 70 µH	2.0 + 1.0 µH [4]	0.2 V	V 4-wire
70 µH to 50 mH	3.0 [1]	0.2 V	V

[1] Error limit: ± % of reading.
Temperature coefficient: ±(0.1 × accuracy) / °C.
[2] V = voltage injection, current measurement.
[3] Min. current limit 20 µA.
[4] Error limit: ±(% of reading + absolute value).
Temperature coefficient: ±(0.1 × accuracy) / °C.
[5] For 1 mH to 2 H: measurement delay = 0.4 × L [s/H].
For 2 H to 100 H: measurement delay = 1 s.

Contact test

R&S®TS-PSAM	
Source voltage	1 V to 5 V
Level	1 kΩ to 1 MΩ

Shorts / continuity test

R&S®TS-PSAM	
Source voltage	0.1 V to 0.5 V
Level	1 Ω to 1 kΩ

Discharge circuit

R&S®TS-PSAM	
Max. input voltage	125 V
Max. discharge current (typ.)	
V > 13 V	10 mA
V < 13 V	150 mA
V < 7 V	300 mA
V < 4.5 V	450 mA

Diode / transistor test

R&S®TS-PSAM, R&S®TS-PICT	
Leakage current	0.1 µA to 100 mA
Forward voltage	0 V to 5 V

Relay multiplexer

R&S®TS-PMB	
Number of pins per module	90
Number of pins per system	900 in R&S®TS-PCA3, 2250 in combination R&S®TS-PCA3 / R&S®TS-PWA3

Analog bus access

R&S®TS-PSAM, R&S®TS-PICT, R&S®TS-PMB	
Analog bus access	8 buses
Max. voltage DC/AC	125 V / 90 V rms
Max. current DC/AC	1 A / 1 A rms
Max. switching power	10 W / 10 VA

General data

Power consumption	
R&S®TS-PSAM	+5 V / 5.8 A, +3.3 V / 0.2 A incl. R&S®TS-PDC, 30 W max.
R&S®TS-PICT	+5 V / 4 A, +3.3 V / 0.2 A incl. R&S®TS-PDC, 25 W max.
R&S®TS-PMB	+5 V / 4.2 A max.
EMC compliance	compliant with EMC directive 89/336/EEC and EMC standard EN 61326
Safety	CE, EN 61010 Part 1
Mechanical loading	
Vibration test, sinusoidal	5 Hz to 55 Hz: 2 g, MIL-T-28800D, class 5, 55 Hz to 150 Hz: 0.5 g, MIL-T-28800D, class 5
Vibration test, random	10 Hz to 300 Hz, 1.2 g
Shock test	40 g, MIL-STD-810, classes 3 and 5
Temperature loading	
Operating range	+5 °C to +40 °C
Permissible range	0 °C to +50 °C
Storage range	–40 °C to +70 °C
Module dimensions in mm	316 × 174 × 20
Weight	
R&S®TS-PSAM	0.75 kg incl. R&S®TS-PDC
R&S®TS-PICT	0.60 kg incl. R&S®TS-PDC
R&S®TS-PMB	0.75 kg
Recommended calibration interval	12 months

Ordering information

Designation	Type	Order No.
Analog Source and Measurement Module	R&S®TS-PSAM	1142.9503.02
In-Circuit Test (ICT) Extension Module	R&S®TS-PICT	1158.0000.02
Switching Matrix Module	R&S®TS-PMB	1143.0039.02
EGTSL Software for ICT Version for R&S®TS-PSAM and -PICT Version for R&S®TS-PSAM only	 R&S®TS-LEGT R&S®TS-LEG2	 1143.4140.02 1166.3992.02
Platform		
R&S®CompactTSVP Test and Measurement Chassis	R&S®TS-PCA3	1152.2518.02
System Controller	R&S®TS-PSC3	1134.2503.06
R&S®PowerTSVP Switching Application Chassis	R&S®TS-PWA3	1157.8043.02
Combination of chassis		
Analog Bus Extension Cable	R&S®TS-PK01	1166.4147.02
CAN Bus Control Cable for extension of R&S®TS-PCA3 with R&S®TS-PWA3	R&S®TS-PK02	1166.4160.02
Test adapter products		
Receiver Frame	R&S®TS-PAD3	1061.8566.02
Connector Carrier for R&S®TS-PAD3 (2 pcs)	R&S®TS-PAX1	1157.9404.02
Fixture Frame	R&S®TS-F3F	1157.9504.02
Connector Carrier for R&S®TS-F3F (5 pcs)	R&S®TS-F3X1	1157.9604.02
Vacuum Control Unit	R&S®TS-PVAC	1166.3970.02

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